



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,886	12/16/2003	Toshio Takayama	031325	5693
23850	7590	12/23/2005	EXAMINER	
ARMSTRONG, KRATZ, QUINTOS, HANSON & BROOKS, LLP			PAREKH, NITIN	
1725 K STREET, NW			ART UNIT	
SUITE 1000			PAPER NUMBER	
WASHINGTON, DC 20006			2811	

DATE MAILED: 12/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

<b>Office Action Summary</b>	<b>Application No.</b>		<b>Applicant(s)</b>	
	10/735,886		TAKAYAMA ET AL.	
	<b>Examiner</b>		<b>Art Unit</b>	
	Nitin Parekh		2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 14 November 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1 and 4-18 is/are pending in the application.
- 4a) Of the above claim(s) 7-17 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1, 4-6 and 18 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

## **DETAILED ACTION**

### ***Request for Continued Examination***

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11-14-05 has been entered. An action on the RCE follows.

### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 4, 6 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takata et al. (US Pat. 6500675).

Regarding claims 1-4, 6 and 18, Takata et al. disclose a semiconductor device (see Fig. 6) having a substrate (1 in Fig. 6) comprising a multilayer interconnection structure (MIS) formed on the substrate, the MIS comprising:

- a first interconnection/electrode layer (FIL- 9b in Fig. 6) including a interconnection pattern made of material such as copper (Col. 9, line 17)
- an interlayer insulation film (11 in Fig. 6) formed on the FIL
- a second interconnection/electrode layer (SIL- 13b in Fig. 6) formed on the interlayer insulation film, the SIL including a interconnection pattern made of material such as aluminum (Col. 9, line 56)
- a via-hole (see the hole filled with 12b in Fig. 6) formed in the interlayer insulation film so as to expose the copper interconnection pattern
- a metal plug formed in the via-hole (12b in Fig. 6) so as to connect the FIL and the SIL electrically, metal plug being formed of a material such as tungsten
- a stacked metal layer/film (see 12a in Fig. 6; Col. 9, lines 50-54) formed between an outer wall of the tungsten plug and an inner wall of the via-hole, the metal layer/film being formed of the stack of conductive nitride layer including a first and second nitride layers such as tantalum nitride (TaN) and titanium nitride (TiN) respectively , and
- the stack of the conductive nitride film being defined by an inner wall contacting with said outer wall of the tungsten plug and an outer wall contacting with the inner wall of the via-hole (Col. 9, lines 50-54), the stack contacting the FIL, and
- the stack structure providing the second nitride film being stacked inside/on the first nitride film, such stacked structure of the first and second metal nitrides (TaN and TiN respectively) being such that outer surface of the first nitride is in

intimate contact with an innerwall of the via-hole and an outer surface of the second nitride being in intimate contact with an inner surface of the first nitride film and an inner surface of the second nitride film being in intimate contact with an outer surface of the tungsten plug

(Fig. 6; Col. 11, line 30- Col. 12, line 40; Col. 7-9; Fig. 1-5).

Takata et al. further teach the via-hole having a high depth/diameter ratio of about 2.0 as seen in Fig. 6, but fail to explicitly teach the depth/diameter ratio being in a range of 1.25-3.0.

The determination of parameters such as via diameter, trench/via depth, aspect ratio (AR), number of vias, spacing/pitch of the vias, number/thickness of interlayer insulating films, etc. including the respective value/range of such dimensions/ratios in the MIS is a subject of routine experimentation and optimization to achieve the desired metal fill characteristics, electrical performance, speed, reduced void/defect level, desired level of integration and improved reliability (see *In re Aller*, 105 USPQ 233).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the via holes having depth/diameter ratio being in a range of 1.25-3.0 so that the metal fill can be improved, the void/defect level can be reduced and the device integration/interconnect reliability can be enhanced in Takata et al's device.

4. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takata et al. (US Pat. 6500675) in view of Brown (US Pat. 6306732).

**A.** Regarding claim 5, Takata et al. teach substantially the entire claimed structure as applied to claim 1 above, except the nitride film having characteristics of being corrosion resistant.

Brown teaches using a multilayered stack of barrier layers having compositions such as TaN and TiN to provide an enhanced/stronger barrier against electromigration/corrosion and stress in an interconnect structure wherein the stack comprises a superior barrier composition such as TaN having the desired composition/structure, thickness and uniformity so that the electromigration/corrosion reliability for the interconnect can be improved and void formation can be reduced (see Col. 12, line 21- Col. 13, line 3; Col. 7-13).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the nitride film showing corrosion resistance as taught by Brown so that the reliability can be improved and the stress related defects/void formation can be reduced in Takata et al's device.

**B.** Regarding claim 5, using the fluoride gaseous source of tungsten for forming the tungsten plug do not distinguish over Takata et al. and Brown, because only the final product/structure is relevant, not forming the tungsten using the "gaseous source",

“plasma source” or “preclean and selective deposition”. Note that a “product by process” claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marrosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a “product by process” claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in “product by process” claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

### ***Response to Arguments***

5. Applicant's arguments filed 11-14-05 have been fully considered but they are not persuasive.

A. Applicant contends that according to Takata et al. teach each nitride film to be accompanied by a metal film part at the bottom part thereof where deposition takes place first in view of the need of avoiding the problem of dust formation explained with reference to Figure 6.

However, such disclosure to use the metal avoiding the problem of dust formation in the structure of Fig. 6 could not be found in Takata et al's reference.

Art Unit: 2811

B. Applicant contends that Brown does not describe the solution for the corrosion problem.

However, as explained in the rejections above, Brown teaches using the metal nitrides such as TaN and TiN to provide an enhanced/stronger barrier against electromigration/corrosion and stress in an interconnect structure, such barrier composition includes TaN having electromigration/corrosion resistant properties so that the reliability for the interconnect can be improved and void formation can be reduced (see Col. 12, line 21- Col. 13, line 3; Col. 7-13).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAN or Public PAG. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAG system, contact the Electronic Business Center



Art Unit: 2811

(EBC) at 866-217-9197 (toll-free). Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

NP

07-03-05



NITIN PAREKH

PRIMARY EXAMINER

TECHNOLOGY CENTER 2800